

6
10/29/01 mclm

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

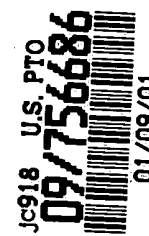
In re application of

Kazuo MATSUZAKI et al.

Serial No.: NEW APPLICATION

Filed: January 9, 2001

For: A SEMICONDUCTOR DEVICE EXHIBITING A HIGH BREAKDOWN VOLTAGE AND
THE METHOD OF MANUFACTURING THE SAME



INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

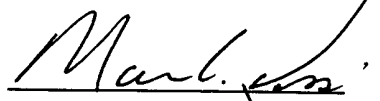
Sir:

Pursuant to 37 C.F.R. §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. Copies of the references listed on Form PTO-1449 are attached. Please note that applicant has enclosed a partial translation of the cited Japanese reference entitled "Lowered on-state resistance of lateral power MOSFET with high withstand voltage for Intelligent Power Device". The translated portion of the article begins on page 21, line 9 from the bottom, to page 23, line 6.

It is respectfully requested that the information be expressly considered during the prosecution of this application, that these references be made of record therein and appear among the "References Cited" on any patent to issue therefrom, and that an initialed copy of the PTO-1449 be returned to the undersigned.

Respectfully submitted,

Date: _____


Marc A. Rossi
Registration No. 31,923

Attorney Docket No.: FUJI:179